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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 2811
Shunpei YAMAZAKI et al.	)	Examiner: S. Hu
Serial No. 09/334,646	)	
Filed: June 17, 1999	)	
For: SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF	)	

CERTIFICATE OF MAILING

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Adele M. Stamper

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 35 U.S.C. § 134 and 37 C.F.R. § 1.192(a), Appellants submit this Appeal Brief in triplicate to appeal the examiner's final rejection of claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52, 53, 58-60, 65, 71-73, 75-81 and 100-121 in the Official Action mailed August 20, 2003.

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I. REAL PARTY IN INTEREST

The named inventors have assigned all ownership rights in the pending application to Semiconductor Energy Laboratory Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken, 243-0036, Japan, which is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

Claims 104-121 were drafted in view of claims 1, 2 and 4 of U.S. Patent No. 6,355,940 to Koga et al. Furthermore, application serial number 09/927,794 is a divisional application based on the '940 patent (Publication Number 2001/0052598 A1), and may still be pending. In the *Preliminary Amendment* filed November 26, 2002, the Appellants noted that the claims "may recite interfering subject matter" and the Appellants requested that the Examiner review the '940 patent and '794 application in connection with the subject application. The potential interference was discussed in an interview and recorded in an *Interview Summary* (Paper No. 33); however, as of the filing of the present *Appeal Brief*, an interference has not been formally acknowledged by the Patent Office. The Appellants have filed under separate cover a *Request by Applicant for Interference with Patent under 37 CFR § 1.607* which formally requests that an interference be declared between the present application and the '940 patent.

Aside from the above, the Appellants, their legal representatives, and the assignee are not aware of any other pending appeals or interferences which will directly affect or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52, 53, 58-60, 65, 71-73, 75-81 and 100-121 are pending in the present application, of which claims 1-3, 8, 104, 107, 110, 113, 116 and 119 are independent. None of the claims have been deemed allowable by the examiner.

IV. STATUS OF AMENDMENTS

All prior amendments are believed to have been entered in the present application. Thus, the status of the claims in this application is as set forth above and in Appendix A.

Please note, a *Request for Acknowledgment of Information Disclosure Statement* has been filed concurrently with the present *Appeal Brief* requesting consideration of the Information Disclosure Statement filed on June 17, 1999, and requesting consideration of a further Information Disclosure Statement filed June 17, 2003.

V. SUMMARY OF THE INVENTION

The present invention relates to an active matrix type display device (e.g. Fig. 6) comprising a plurality of pixels (e.g. page 22, ¶2) arranged in matrix form over a substrate (e.g. substrate 15, page 22, ¶2); a driver circuit (e.g. X decoder/driver, Y decoder/driver) for driving the plurality of pixels over the substrate, the driver circuit may include at least one buffer circuit (e.g. Fig. 3, page 22, ¶2); at least two transistors (e.g. upper, middle and lower transistors in Fig. 3, see also page 21, ¶3) in the at least one buffer circuit or in the driver circuit; a common gate wiring (e.g. common gate electrode and gate wiring 108, Fig. 3, page 21, ¶1) connected with the at least two transistors at gate electrodes (e.g. gate electrode 108, Fig. 3, pages 15-16) of the at least two transistors; a common source wiring (e.g. common source electrode and source wiring 116, Fig. 3, page 21, ¶1) connected with the at least two transistors at one of a source (e.g. source region 110, Fig. 1C, page 16) and a drain (e.g. drain region 114, Id.) of each of the at least two transistors; a common drain wiring (e.g. common drain electrode and drain wiring 117, Fig. 3, page 21, ¶1) connected with the at least two transistors at the other of the source and drain of each of the at least two transistors; where the at least two transistors are connected with each other in parallel (e.g. Fig. 3, top of page 11 to top of page 13; and bottom of page 19 to bottom of page 21) by the connections of the common gate wiring, the common source wiring, and the common drain wiring with the at least two transistors (e.g. Fig. 3); where channel-forming regions (e.g. channel-forming region 112, the top of page 15 to the top of page 16, page 19, ¶1 to page 20, ¶2) of the at least two transistors are separately provided in at least two separate semiconductor layers respectively (e.g. Fig. 3), and each of the channel-forming regions may be provided such that they do not have linear defects or surface defects (page 8, ¶2).

The present invention also relates to a display device (e.g. Fig. 6, see also page 1, line 12) comprising a plurality of pixel electrodes (e.g. page 22, ¶2) formed on or over a

substrate (e.g. substrate 15, page 22, ¶2, see also Fig. 6); a plurality of first thin film transistors (e.g. TFT 11, page 22, ¶2), which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal (e.g. Embodiment 4, pages 22-23, see also Fig. 6); and a plurality of second thin film transistors (e.g. upper, middle and lower transistors in Fig. 3, see also page 21, ¶3), which configure a driving circuit (e.g. X decoder/driver, Y decoder/driver) for driving the plurality of first thin film transistors (see also page 2, lines 21-22); where (some of or at least one of) the plurality of second thin film transistors each has a plurality of channel areas (e.g. channel-forming region 112, the top of page 16 to the top of page 17, page 20, ¶1 to page 21, ¶2) formed in a semiconductor layer subjected to laser annealing respectively (e.g. page 16, ¶1, see also Figs. 1A and 3, and page 21, ¶2), and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel (e.g. Fig. 3, top of page 11 to top of page 13; and bottom of page 19 to bottom of page 21) to each other and arranged separately (e.g. Fig. 3).

VI. STATEMENT OF ISSUES

A. Whether claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52, 53, 58-60, 65, 71-73, 75-81 and 100-103 are not *prima facie* obvious based on the combination of U.S. Patent No. 5,403,772 to Zhang et al., U.S. Patent No. 5,233,447 to Kuribayashi et al., and U.S. Patent No. 5,173,792 to Matsueda.

B. Whether claims 104-121 are not *prima facie* obvious based on the combination of Zhang and Matsueda.

VII. GROUPING OF CLAIMS

The claims do not stand or fall together. The Appellants appeal the grounds of rejection for two groups of claims. The first group includes claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52, 53, 58-60, 65, 71-73, 75-81 and 100-103. The second group includes

claims 104-121. In the arguments below, the Appellants provide reasons why the claims of each group are believed to be separately patentable.

VIII. ARGUMENTS

A. Whether claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52, 53, 58-60, 65, 71-73, 75-81 and 100-103 are not *prima facie* obvious based on the combination of U.S. Patent No. 5,403,772 to Zhang et al., U.S. Patent No. 5,233,447 to Kuribayashi et al., and U.S. Patent No. 5,173,792 to Matsueda.

Paragraph 7 of the final Official Action rejects claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52, 53, 58-60, 65, 71-73, 75-81 and 100-103 as obvious based on the combination of U.S. Patent No. 5,403,772 to Zhang et al., U.S. Patent No. 5,233,447 to Kuribayashi et al., and U.S. Patent No. 5,173,792 to Matsueda. The Appellants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

It is respectfully submitted that the Official Action has failed to establish a *prima facie* case of obviousness in that one of skill in the art would not have been motivated to combine the teachings of Zhang, Kuribayashi and Matsueda to achieve the present invention.

As noted in detail above, the present invention relates to an active matrix type display device comprising a plurality of pixels arranged in matrix form over a substrate; a driver circuit for driving the plurality of pixels over the substrate, the driver circuit may include at least one buffer circuit; at least two transistors in the at least one buffer circuit or in the driver circuit; a common gate wiring connected with the at least two transistors at gate electrodes of the at least two transistors; a common source wiring connected with the at least two transistors at one of a source and a drain of each of the at least two transistors; a common drain wiring connected with the at least two transistors at the other of the source and drain of each of the at least two transistors; where the at least two transistors are connected with each other in parallel by the connections of the common gate wiring, the common source wiring, and the common drain wiring with the at least two transistors; where channel-forming regions of the at least two transistors are separately provided in at least two separate semiconductor layers respectively, and each of the channel-forming regions may be provided such that they do not have linear defects or surface defects.

Zhang appears to teach in Fig. 8(A) a display device with a data driver 101, a gate driver 102, an active matrix 103 connected through gate lines 105 and data lines 106 on an insulating substrate 107. Very little discussion is given to the data driver 101 and the gate driver 102 of Zhang. At best, it appears that Zhang discloses that it is desirable to provide a cover film on the peripheral circuit region to turn it into high mobility TFTs (column 9, lines 47-55). As noted above, Zhang does not specifically discuss the structure of the data driver 101 and the gate driver 102; however, the Official Action refers to the structure in Fig. 3(A) and asserts that "thin film transistors (TFTs) in the driver circuit portion each having a channel forming region in one of the separate semiconductor layers (11a and 11b) provided on an insulating surface" (page 4, Paper No. 38). It is not clear that the structure of Fig. 3(A) is necessarily the structure of the data driver 101 and the gate driver 102.

The Official Action concedes that Zhang does not teach "that the peripheral driver circuit portion comprises at least two TFTs connected in parallel" (page 5, Paper No. 38). Although not explicitly stated in the Official Action, Zhang also does not teach or suggest that the peripheral driver circuit portion comprises at least two transistors connected in parallel by connections of a common gate wiring, a common source wiring, and a common drain wiring with the at least two transistors or that the channel-forming regions of the at least two transistors are separately provided in at least two separate semiconductor layers respectively. The Official Action relies on Matsueda to allegedly teach the above features and asserts that it would have been obvious to combine Matsueda with Zhang.

The Official Action further asserts that Matsueda teaches that the reliability of a basic control element comprising two or more parallel-connected TFTs is better than that of a basic control element comprising a single TFT. The Official Action thus concludes that one of skill in the art would readily recognize that the reliability of the buffer circuit and/or other peripheral circuits in the active matrix type LC display device of Zhang would also be improved if the basic transistor in the buffer circuit and/or other peripheral circuits is formed of two or more parallel-connected TFTs.

The Appellants respectfully disagree with the above assertions for the reasons stated below. Matsueda appears to disclose TFTs 100A and 100B provided at respective pixel portions of the display device, which is not related to the buffer circuit or driver circuit of the claimed invention. Particularly, it is noted that Matsueda teaches two parallel-connected TFTs (100A and 100B) in Fig. 7 so that either one of the TFTs can be cut off at portions 113 and 114 if it is found to be defective (column 13, line 57 to column 14, line 13). There is no teaching or suggestion in Matsueda or the prior art to indicate how or why one of ordinary skill would remove the pixel driving TFTs 100A and 100B of Matsueda and be motivated to insert them into the display device of Zhang, much less specifically replace the data driver 101 and/or the gate driver 102 of Zhang with TFTs 100A and 100B of Matsueda. It is also unclear how or why one of ordinary skill in the art would combine the driving electrode 101, the gate wire 102 and the signal line X_m of Matsueda as a means for connecting TFTs 100A and 100B in the device of Zhang. It is also unclear in the alleged combined device of Zhang and Matsueda

whether one would use the allegedly monocrystalline semiconductor regions 11a and 11b shown in Fig. 3(A) of Zhang, the TFTs of Matsueda, or some hypothetical combination of the two. It appears that one would need to completely redesign the connections of the Matsueda TFTs, which are provided at respective pixel portions of the display device, in order to convert such TFTs for use as a buffer or driver circuit of a display device, and such a redesign is not taught or suggested by the prior art and would not have been known to one of ordinary skill in the art at the time of the invention.

Matsueda is concerned about a specific problem unique to the pixel portion of an electrooptical display and is silent about the peripheral portion, buffer circuit or driver circuit as disclosed in the present invention. Neither Matsueda, nor the other prior art of record, discloses or suggests any problem with the prior art peripheral portion, buffer circuit or driver circuit and thus one of skill in the art would not have been motivated to modify such circuits to include parallel connected TFTs. Zhang and Matsueda are silent concerning any problem with reliability in the driver circuit or in a driver circuit comprising a buffer circuit. While the Official Action asserts that such parallel connection would provide greater reliability and thus would be used in a buffer circuit and/or other peripheral circuits, there is no disclosure or suggestion that reliability in such circuits is a problem or that such parallel interconnection of TFTs could solve such problem if it even existed.

Furthermore, the Appellants have recognized a problem in prior art buffer and driver circuits concerning excess heat caused by a large current in the buffer or driver circuit as described, for example, on page 19, lines 11-29. The present invention is based on a recognition of the problem caused by this excess heat in the buffer or driver circuit, and the Appellants discovered that the problem could be solved when channel-forming regions of at least two transistors in the buffer or driver circuit of a display device are separately provided in at least two separate semiconductor layers respectively, as shown in Fig. 3. Please note that independent claims 1-3 and 8 recite precisely this feature. The Appellants have recognized a specific problem that occurs in the buffer or driver circuit and have presented a solution by the present invention. The prior art of record does not recognize this problem. Therefore, one of ordinary skill in

the art would not have been motivated by the teachings of Zhang and Matsueda, or any of the prior art of record, to form a buffer or driver circuit where channel-forming regions of at least two transistors in the buffer or driver circuit are separately provided in at least two separate semiconductor layers respectively, as shown in Fig. 3.

The Official Action asserts that the fact that Appellants have recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. It is respectfully submitted, however, that there is no suggestion in the prior art and, absent the recognition of the problem discovered by the Appellants, one of skill in the art would not be motivated to replace the buffer or driver circuit of the prior art with the pixel circuit of Matsueda.

Furthermore, the fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). See MPEP § 2143.01. It is respectfully submitted that the teachings of Matsueda are insufficient to teach or suggest to one of skill in the art that the buffer circuit should include parallel connected TFTs.

Also, the assertion that reliability is always a problem and that "Matsueda teaches that the reliability of a basic control element comprising two or more parallel-connected TFTs is better than that of a basic control element comprising a single TFT" (page 5, Paper No. 38) is overly broad. Assuming the Examiner is correct, one would be led to presume that it is always obvious to connect any circuit in parallel. The Appellants respectfully submit that there would be no reasonable expectation of success which would support the assertion that circuits should always be connected in parallel in order to improve reliability.

Furthermore, Matsueda is not concerned with a "basic control element" but rather is concerned with a specific problem concerning defective display element circuits. Column 1, lines 6-14 make this clear, stating:

> The invention relates to electrooptical displays and more particularly to active matrix type electrooptical displays with redundant

> means to provide for substantially complete relief from defective circuits of display elements, also referred to in the art as picture elements or pixels. The built-in redundancy provides a means to correct for defective display element circuits in the fabricated display thereby increasing their manufacturing yield.

Kuribayashi does not cure the deficiencies in the motivation to combine Zhang and Matsueda. The Official Action relies on Kuribayashi to allegedly teach a buffer circuit in a driver circuit (page 5, Paper No. 38). Kuribayashi does not show how or why one of ordinary skill would remove the pixel driving TFTs 100A and 100B of Matsueda and be motivated to insert them into the display device of Zhang, much less specifically replace the data driver 101 and/or the gate driver 102 of Zhang with TFTs 100A and 100B of Matsueda.

For all of the above reasons, it is respectfully submitted that one of skill in the art would not have been motivated to combine the references as asserted in the Official Action to achieve the present invention. A *prima facie* case of obviousness cannot be maintained and reconsideration is requested.

The Appellants also respectfully submit that claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52, 53, 58-60, 65, 71-73, 75-81 and 100-103 are patentably distinct from claims 104-121. Independent claims 104, 107, 110, 113, 116 and 119 recite the following features which are not taught or suggested in independent claims 1-3 and 8: (some of or at least one of) a plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively. Also, independent claims 1-3 and 8 recite the following features which are not taught or suggested in claims 104-121: a common gate wiring connected with the at least two transistors at gate electrodes of the at least two transistors; a common source wiring connected with the at least two transistors at one of a source and a drain of each of the at least two transistors; a common drain wiring connected with the at least two transistors at the other of the source and drain of each of the at least two transistors; where the at least two transistors are connected with each other in parallel by the connections of the common gate wiring, the common source wiring, and the common drain wiring with the at least two transistors. Also, independent claims 1 and 3 recite the

following features which are not taught or suggested in claims 104-121: a driver circuit including at least one buffer circuit; at least two transistors in the at least one buffer circuit. Therefore, the Appellants respectfully submit that claims 1-3, 8, 11-14, 16-19, 32-34, 38-43, 52, 53, 58-60, 65, 71-73, 75-81 and 100-103 are patentably distinct from claims 104-121.

B. Whether claims 104-121 are not *prima facie* obvious based on the combination of Zhang and Matsueda.

Paragraph 8 of the Official Action rejects claims 104-121 as obvious based on the combination of Zhang and Matsueda. The Appellants respectfully traverse the rejection because the Official Action has not made a *prima facie* case of obviousness.

Initially, the Applicants respectfully submit that the rejection of claims 104-121 is not proper in that claims 104-121 are substantially similar to the claims of an issued patent, and in that the rejection fails to include the approval of the TC Director. It is noted that claims 104-121 are substantially identical to claims 1, 2 and 4 of U.S. Patent No. 6,355,940 to Koga et al. While claims 104-121 are not verbatim copies of claims 1, 2 and 4 of Koga, the differences between claims 104-121 and claims 1, 2 and 4 of Koga are irrelevant to the alleged basis for the rejection. The rejection, if valid, would necessarily apply equally to the claims of Koga. Therefore, it appears that the alleged ground of rejection of claims 104-121 would also apply to at least claims 1, 2 and 4 of the Koga patent. As noted in MPEP § 2307.02, "If the ground of rejection is also applicable to the corresponding claims in the patent, any letter including the rejection must have the approval of the TC Director." It does not appear that the present rejection includes the approval of the TC Director. Reconsideration of the rejection under § 103 is requested.

As noted in detail above, the present invention also relates to a display device comprising a plurality of pixel electrodes formed on or over a substrate; a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; where (some of or at least one of) the plurality of second thin film transistors each has a plurality of

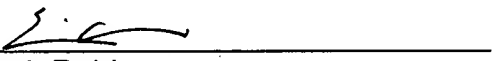
channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

For the same reasons as stressed above, it is respectfully submitted that the Official Action has failed to provide a sufficient basis to show that one of skill in the art would have been motivated to combine Zhang and Matsueda to achieve the present invention and thus a *prima facie* case of obviousness cannot be maintained. Favorable reconsideration is requested.

Paragraph 3 of the Official Action objects to claims 104, 107, 110, 113, 116, and 119 for a number of minor informalities. In response, the Appellants respectfully request reconsideration. It is noted that the language objected to by the Examiner is included in issued U.S. Patent No. 6,355,940. In that this language is included in the issued '940 patent, it is believed to be unobjectionable and it is respectfully requested that the objections be withdrawn. Reconsideration is requested.

The present application is believed to be in condition for allowance and favorable reconsideration is respectfully requested. If the Examiner feels further discussions would expedite prosecution of this application, he is invited to contact the undersigned.

Respectfully submitted,



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IX. APPENDICES

A. Claims involved in the appeal.

B. U.S. Patent No. 5,403,772 to Zhang et al.

C. U.S. Patent No. 5,233,447 to Kuribayashi et al.

D. U.S. Patent No. 5,173,792 to Matsueda.

APPENDIX A

PENDING CLAIMS

1. An active matrix type display device comprising:

a plurality of pixels arranged in matrix form over a substrate;

a driver circuit for driving the plurality of pixels over said substrate, said driver circuit including at least one buffer circuit;

at least two transistors in said at least one buffer circuit;

a common gate wiring connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively.

2. An active matrix type display device comprising:

a plurality of pixels arranged in matrix form over a substrate;

a driver circuit for driving the plurality of pixels over said substrate;

at least two transistors in said driver circuit;

a common gate wiring connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively.

3. An active matrix type display device comprising:

a plurality of pixels arranged in matrix form over a substrate;

a driver circuit for driving the plurality of pixels over said substrate, said driver circuit including at least one buffer circuit;

at least two transistors in said at least one buffer circuit;

a common gate wiring connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively and each of said channel-forming regions not having linear defects or surface defects.

8. An active matrix type display device comprising:

a plurality of pixels arranged in matrix form over a substrate;

a driver circuit for driving the plurality of pixels over said substrate;

at least two transistors in said driver circuit in said active matrix type display device;

a common gate wiring connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively and each of said channel-forming regions not having linear defects or surface defects.

11. The device of claim 1 wherein said active matrix type display device comprises a memory.

12. The device of claim 1 wherein said active matrix type display device comprises a decoder.

13. The device of claim 1 wherein said active matrix type display device comprises a display system.

14. The device of claim 2, wherein said active matrix type display device comprises a memory.

16. The device of claim 2 wherein said active matrix type display device comprises a display system.

17. The device of claim 3 wherein said active matrix type display device comprises a memory.

18. The device of claim 3 wherein said active matrix type display device comprises a decoder.

19. The device of claim 3 wherein said active matrix type display device comprises a display system.

32. The device of claim 8 wherein said active matrix type display device comprises a memory.

33. The device of claim 8 wherein said active matrix type display device comprises a decoder.

34. The device of claim 8 wherein said active matrix type display device comprises a display system.

38. The device of claim 58 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

39. The device of claim 58 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

40. The device of claim 59 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

41. The device of claim 59 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

42. The device of claim 60 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

43. The device of claim 60 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

52. The device of claim 65 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

53. The device of claim 65 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

58. The device of claim 1 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

59. The device of claim 2 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

60. The device of claim 3 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being

effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

65. The device of claim 8 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

71. The device of claim 1 wherein said active matrix type display device is a liquid crystal display device.

72. The device of claim 2 wherein said active matrix type display device is a liquid crystal display device.

73. The device of claim 3 wherein said active matrix type display device is a liquid crystal display device.

75. The device of claim 8 wherein said active matrix type display device is a liquid crystal display device.

76. The device of claim 1 wherein said channel-forming region does not have linear defects or surface defects.

77. The device of claim 2 wherein said channel-forming region does not have linear defects or surface defects.

78. The device of claim 1 wherein said channel-forming region has point defects.

79. The device of claim 2 wherein said channel-forming region has point defects.

80. The device of claim 3 wherein said channel-forming region has point defects.

81. The device of claim 8 wherein said channel-forming region has point defects.

100. The device of claim 1, wherein each of said channel-forming regions contains carbon and nitrogen at a concentration of 5×10^{18} cm^{-3} or less, respectively, and contains oxygen at a concentration of 5×10^{19} cm^{-3} or less.

101. The device of claim 2, wherein each of said channel-forming regions contains carbon and nitrogen at a concentration of 5×10^{18} cm^{-3} or less, respectively, and contains oxygen at a concentration of 5×10^{19} cm^{-3} or less.

102. The device of claim 3, wherein each of said channel-forming regions contains carbon and nitrogen at a concentration of 5×10^{18} cm^{-3} or less, respectively, and contains oxygen at a concentration of 5×10^{19} cm^{-3} or less.

103. The device of claim 8, wherein each of said channel-forming regions contains carbon and nitrogen at a concentration of 5×10^{18} cm^{-3} or less, respectively, and contains oxygen at a concentration of 5×10^{19} cm^{-3} or less.

104. A display device, comprising:

a plurality of pixel electrodes formed on a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

the plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

105. The display device according to claim 104, wherein the plurality of channel areas are separated in a direction of the channel width.

106. The display device according to claim 104, wherein the laser annealing is performed to crystallize an amorphous semiconductor layer in order to obtain a crystalline semiconductor layer.

107. A display device, comprising:

a plurality of pixel electrodes formed on a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein

some of the plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

108. The display device according to claim 107, wherein the plurality of channel areas are separated in a direction of the channel width.

109. The display device according to claim 107, wherein the laser annealing is performed to crystallize an amorphous semiconductor layer in order to obtain a crystalline semiconductor layer.

110. A display device, comprising:

a plurality of pixel electrodes formed on a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

at least one of the plurality of second thin film transistors has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

111. The display device according to claim 110, wherein the plurality of channel areas are separated in a direction of the channel width.

112. The display device according to claim 110, wherein the laser annealing is performed to crystallize an amorphous semiconductor layer in order to obtain a crystalline semiconductor layer.

113. A display device, comprising:

a plurality of pixel electrodes formed over a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

the plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

114. The display device according to claim 113, wherein the plurality of channel areas are separated in a direction of the channel width.

115. The display device according to claim 113, wherein the laser annealing is performed to crystallize an amorphous semiconductor layer in order to obtain a crystalline semiconductor layer.

116. A display device, comprising:

a plurality of pixel electrodes formed over a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

some of the plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

117. The display device according to claim 116, wherein the plurality of channel areas are separated in a direction of the channel width.

118. The display device according to claim 116, wherein the laser annealing is performed to crystallize an amorphous semiconductor layer in order to obtain a crystalline semiconductor layer.

119. A display device, comprising:

a plurality of pixel electrodes formed over a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

at least one of the plurality of second thin film transistors has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing

respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

120. The display device according to claim 119, wherein the plurality of channel areas are separated in a direction of the channel width.

121. The display device according to claim 119, wherein the laser annealing is performed to crystallize an amorphous semiconductor layer in order to obtain a crystalline semiconductor layer.

IX. APPENDICES

A. Claims involved in the appeal.

B. U.S. Patent No. 5,403,772 to Zhang et al.

C. U.S. Patent No. 5,233,447 to Kuribayashi et al.

D. U.S. Patent No. 5,173,792 to Matsueda.

APPENDIX A

PENDING CLAIMS

1. An active matrix type display device comprising:

a plurality of pixels arranged in matrix form over a substrate;

a driver circuit for driving the plurality of pixels over said substrate, said driver circuit including at least one buffer circuit;

at least two transistors in said at least one buffer circuit;

a common gate wiring connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively.

2. An active matrix type display device comprising:

a plurality of pixels arranged in matrix form over a substrate;

a driver circuit for driving the plurality of pixels over said substrate;

at least two transistors in said driver circuit;

a common gate wiring connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively.

3. An active matrix type display device comprising:

a plurality of pixels arranged in matrix form over a substrate;

a driver circuit for driving the plurality of pixels over said substrate, said driver circuit including at least one buffer circuit;

at least two transistors in said at least one buffer circuit;

a common gate wiring connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring, and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively and each of said channel-forming regions not having linear defects or surface defects.

8. An active matrix type display device comprising:

a plurality of pixels arranged in matrix form over a substrate;

a driver circuit for driving the plurality of pixels over said substrate;

at least two transistors in said driver circuit in said active matrix type display device;

a common gate wiring connected with said at least two transistors at gate electrodes of said at least two transistors;

a common source wiring connected with said at least two transistors at one of source and drain of each of said at least two transistors;

a common drain wiring connected with said at least two transistors at the other of the source and drain of each of said at least two transistors,

wherein said at least two transistors are connected with each other in parallel by the connections of said common gate wiring, said common source wiring and said common drain wiring with said at least two transistors, and

wherein channel-forming regions of said at least two transistors are separately provided in at least two separate semiconductor layers respectively and each of said channel-forming regions not having linear defects or surface defects.

11. The device of claim 1 wherein said active matrix type display device comprises a memory.

12. The device of claim 1 wherein said active matrix type display device comprises a decoder.

13. The device of claim 1 wherein said active matrix type display device comprises a display system.

14. The device of claim 2, wherein said active matrix type display device comprises a memory.

16. The device of claim 2 wherein said active matrix type display device comprises a display system.

17. The device of claim 3 wherein said active matrix type display device comprises a memory.

18. The device of claim 3 wherein said active matrix type display device comprises a decoder.

19. The device of claim 3 wherein said active matrix type display device comprises a display system.

32. The device of claim 8 wherein said active matrix type display device comprises a memory.

33. The device of claim 8 wherein said active matrix type display device comprises a decoder.

34. The device of claim 8 wherein said active matrix type display device comprises a display system.

38. The device of claim 58 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

39. The device of claim 58 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

40. The device of claim 59 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

41. The device of claim 59 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

42. The device of claim 60 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

43. The device of claim 60 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

52. The device of claim 65 wherein ratio (W/W_0) between width W_0 of a spectrum at a position at half of a Raman spectrum intensity for a monocrystalline silicon wafer and a width W of a spectrum at a position at half of a Raman spectrum intensity for said regions which can be regarded as being effectively monocrystalline is 2.0 or less.

53. The device of claim 65 wherein ratio (I/I_0) between a Raman spectrum intensity I_0 of a monocrystalline silicon wafer and a Raman spectrum intensity I of said regions which can be regarded as being effectively monocrystalline is 0.8 or more.

58. The device of claim 1 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

59. The device of claim 2 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

60. The device of claim 3 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being

effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

65. The device of claim 8 wherein at least said channel-forming regions of said at least two transistors are provided in regions which can be regarded as being effectively monocrystalline, and wherein said regions which can be regarded as being effectively monocrystalline comprise silicon.

71. The device of claim 1 wherein said active matrix type display device is a liquid crystal display device.

72. The device of claim 2 wherein said active matrix type display device is a liquid crystal display device.

73. The device of claim 3 wherein said active matrix type display device is a liquid crystal display device.

75. The device of claim 8 wherein said active matrix type display device is a liquid crystal display device.

76. The device of claim 1 wherein said channel-forming region does not have linear defects or surface defects.

77. The device of claim 2 wherein said channel-forming region does not have linear defects or surface defects.

78. The device of claim 1 wherein said channel-forming region has point defects.

79. The device of claim 2 wherein said channel-forming region has point defects.

80. The device of claim 3 wherein said channel-forming region has point defects.

81. The device of claim 8 wherein said channel-forming region has point defects.

100. The device of claim 1, wherein each of said channel-forming regions contains carbon and nitrogen at a concentration of 5×10^{18} cm^{-3} or less, respectively, and contains oxygen at a concentration of 5×10^{19} cm^{-3} or less.

101. The device of claim 2, wherein each of said channel-forming regions contains carbon and nitrogen at a concentration of 5×10^{18} cm^{-3} or less, respectively, and contains oxygen at a concentration of 5×10^{19} cm^{-3} or less.

102. The device of claim 3, wherein each of said channel-forming regions contains carbon and nitrogen at a concentration of 5×10^{18} cm^{-3} or less, respectively, and contains oxygen at a concentration of 5×10^{19} cm^{-3} or less.

103. The device of claim 8, wherein each of said channel-forming regions contains carbon and nitrogen at a concentration of 5×10^{18} cm^{-3} or less, respectively, and contains oxygen at a concentration of 5×10^{19} cm^{-3} or less.

104. A display device, comprising:

a plurality of pixel electrodes formed on a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

the plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

105. The display device according to claim 104, wherein the plurality of channel areas are separated in a direction of the channel width.

106. The display device according to claim 104, wherein the laser annealing is performed to crystallize an amorphous semiconductor layer in order to obtain a crystalline semiconductor layer.

107. A display device, comprising:

a plurality of pixel electrodes formed on a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein

some of the plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

108. The display device according to claim 107, wherein the plurality of channel areas are separated in a direction of the channel width.

109. The display device according to claim 107, wherein the laser annealing is performed to crystallize an amorphous semiconductor layer in order to obtain a crystalline semiconductor layer.

110. A display device, comprising:

a plurality of pixel electrodes formed on a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

at least one of the plurality of second thin film transistors has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

111. The display device according to claim 110, wherein the plurality of channel areas are separated in a direction of the channel width.

112. The display device according to claim 110, wherein the laser annealing is performed to crystallize an amorphous semiconductor layer in order to obtain a crystalline semiconductor layer.

113. A display device, comprising:

a plurality of pixel electrodes formed over a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

the plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

114. The display device according to claim 113, wherein the plurality of channel areas are separated in a direction of the channel width.

115. The display device according to claim 113, wherein the laser annealing is performed to crystallize an amorphous semiconductor layer in order to obtain a crystalline semiconductor layer.

116. A display device, comprising:

a plurality of pixel electrodes formed over a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

some of the plurality of second thin film transistors each has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

117. The display device according to claim 116, wherein the plurality of channel areas are separated in a direction of the channel width.

118. The display device according to claim 116, wherein the laser annealing is performed to crystallize an amorphous semiconductor layer in order to obtain a crystalline semiconductor layer.

119. A display device, comprising:

a plurality of pixel electrodes formed over a substrate;

a plurality of first thin film transistors, which are connected to corresponding pixel electrodes among the plurality of pixel electrodes and respectively supply the connected corresponding pixel electrode with a display signal; and

a plurality of second thin film transistors, which configure a driving circuit for driving the plurality of first thin film transistors; wherein,

at least one of the plurality of second thin film transistors has a plurality of channel areas formed in a semiconductor layer subjected to laser annealing

respectively, and the plurality of channel areas of each respective second thin film transistor are electrically connected in parallel to each other and arranged separately.

120. The display device according to claim 119, wherein the plurality of channel areas are separated in a direction of the channel width.

121. The display device according to claim 119, wherein the laser annealing is performed to crystallize an amorphous semiconductor layer in order to obtain a crystalline semiconductor layer.